

REMARKS

The present amendment is intended to be fully responsive to all points of rejection raised by the Examiner in the parent application and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt reconsideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1, 4, 5 and 7 through 12 are pending in the application. Claims 1, 4, 5 and 7 through 12 have been rejected. Claims 1, 4, 5 and 7 have been amended to clarify the present invention in comparison to the cited reference.

35 U.S.C. 102 Rejections

Claims 1, 4, 5 and 7 to 12 stand rejected under 35U.S.C .102(e) as being anticipated by Aloni - US 6,346,442. In view of the clarification of claims 1, 4, 5 and 7 provided by the amendments to these claims introduced in the present correspondence, Applicant respectfully requests withdrawal of the above mentioned 102 rejections. More specifically, claims 1, 4, 5 and 7 have been amended to replace the term "retention" with the term "localization", which term more clearly points out the distinction between the teachings of the Aloni reference and the claimed method.

The Aloni reference teaches:

"A fieldless array of floating gate transistors is fabricated by forming an oxide-nitride-oxide (ONO) layer over a semiconductor substrate. A mask is formed over the ONO layer, the mask having openings that define a plurality of bit line regions of the floating gate transistors in the substrate. A first impurity is implanted into the bit line regions of the substrate, wherein the first impurity is implanted through the ONO layer, through the openings of the mask. The first impurity is implanted at various angles, such that the first impurity is implanted in the substrate at locations beneath

the mask. The upper oxide and nitride layers of the ONO layer are subsequently etched through the mask openings. A second impurity is implanted in the substrate through the openings of the mask. The mask is removed, and the substrate is oxidized, thereby forming bit line oxide regions over the bit line regions, and floating gate structures. A plurality of gate electrodes are formed over the bit line oxide regions and the floating gate structures, thereby completing the fieldless array of floating gate transistors. Process steps are also provided for fabricating high voltage and low voltage CMOS transistors on the same wafer as the fieldless array. "

The transistors taught in the Aloni reference are single bit transistors which may use the nitride within an oxide-nitride-oxide sandwich to retain charge. Aloni also mentions that an oxide layer may assist in retaining charge within the nitride layer. That is, the oxide on both sides of the nitride may assist in keeping charge from escaping the nitride layer. Aloni makes no reference or suggestion to keeping charge localized within specific regions of the nitride layer. As a matter of fact, by referring to the memory cells as "floating gate" cells, Aloni implies that the charge retained within the nitride layer of its memory cells is free move around the nitride layer.

Aloni also mentions at least two methods of applying the oxide layer, (1) oxidation of the nitride layer and (2) oxide deposition on the nitride. There is no specific mention of "causing oxygen to be introduced into substantially all of said nitride layer" according to either of the taught methods. Especially according to the second method, there does not seem be any substantial quantity of oxygen introduced into the nitride.

Contrary to what is taught or suggested by the Aloni reference, each of the independent claims 1, 4, 5 and 7, includes the limitation of introducing oxygen into substantially all of a nitride layer within said memory cell, so as to enhance charge localization within said nitride layer. Localization is a limitation of the claimed method because the cells produced by the claimed method may have at least two charge storage regions within each nitride layer, thereby facilitating the storage of multiple bits per memory cell, when required. The Aloni reference does not mention or suggest having memory cells with multiple charge storage regions within the nitride layer and thus no mention is made of introducing oxygen into the nitride so as to enhance charge localization within regions of the nitride. The only mentioned use of oxygen in the Aloni reference is to form oxide layers which surround the nitride layer and assist in retaining charge generally within the nitride

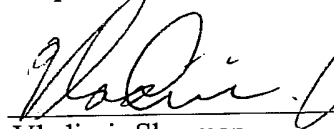
layer. No mention or suggestion is made in the Aloni reference of using oxygen (oxidation or oxide deposition) in limiting the movement of charge within specific regions of the nitride layer (e.g. localization).

In view of the foregoing amendments and remarks, the independent claims 1, 4, 5 and 7 are believed to be allowable. Their favorable reconsideration and allowance is respectfully requested. Furthermore, all claims depending from claims 1, 4, 5 and 7 should now also be allowable by virtue of their dependency from allowable base claims. Their favorable reconsideration and allowance is also respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit Account No. 05-0649.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Kindly amend claims 1, 4, 5 and 7 as follows:

1. (Trice amended) A method of fabricating an oxide-nitride-oxide (ONO) layer in a memory cell, said method comprising:

forming a bottom oxide layer on a substrate;

depositing a nitride layer; and

oxidizing a top oxide layer, thereby causing oxygen to be introduced into substantially all of said nitride layer within said memory cell, so as to enhance charge [retention] localization within said nitride layer.

4. (Trice amended) A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer; and

introducing oxygen into substantially all of said nitride layer within said memory cell, so as to enhance charge [retention] localization within said nitride layer.

5. (Trice amended) A method for improving the charge retention in a nitride layer of a memory cell, said method comprising:

depositing a nitride layer;

controlling the thickness of said deposited nitride layer; and

introducing oxygen into substantially all of said nitride layer within said memory cell, so as to enhance charge [retention] localization within said nitride layer.

7. (Twice amended) A method of manufacturing a programmable, read only memory device, the method comprising:

forming a first oxide layer on a substrate,

forming a nitride layer on top of said oxide layer, wherein said nitride layer is 150 angstroms or less thick;

introducing oxygen into substantially all of said nitride layer within a memory cell during formation of a second oxide layer on top of said nitride layer, so as to enhance charge [retention] localization within said nitride layer;

patterning said oxide-nitride-oxide (ONO) layers into desired patterns; and
forming a gate layer over said patterned ONO layer.